Instructions on FPGA Board and Xilinx software

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I. XILINX AND FPGA INTRODUCTION

Field-Programmable Gate Array (FPGA) - A logic chip which can be programmed to function as an array of computational logic blocks.

Xilinx Software - Xilinx Software allows a designer to graphically create a logic circuit which can be tested and simulated prior to implementation on the FPGA board.

FPGA vs Breadboarding [1]

- FPGA's simplify design, implementation, testing, and debugging
- Reusable - Easily reprogrammed and reconfigured
- Most are non volatile
- Useful in prototyping IC designs
- Low power
- High number of gates/parts in the same area
- HDL helps create libraries (new gates or parts) and functional blocks
- Do not need to worry about voltage, current, or power to each gate or circuit part
- Circuit can be simulated and debugged before implementation; therefore saving time and money

FPGAs can be programmed using schematics to lay out a design, or by using an HDL like Verilog or VHDL. As well as being cheap to program for an application, FPGA hardware is relatively inexpensive. FPGAs can be used for complex applications, such as image processing or image compression, and are suitable for use in portable phones, digital cameras, and other complex digital applications. Xilinx, as well as other companies sell intellectual property (IP) cores, and opencores.org provides cores and source code for free under the GPL.

Evaluating the performance of an FPGA is difficult. Most manufacturers don't provide a gate count for their products, because it tends to be misleading. Mostly, FPGA manufacturers give a number of "logic units" or "logic cells," which consist of a lookup table and a flip-flop, as well as assorted connection logic.

Because different manufacturers use different types of basic gates (AND vs. NAND, etc), the gate count of a logic unit isn't the same across different manufacturers, or even different FPGAs.

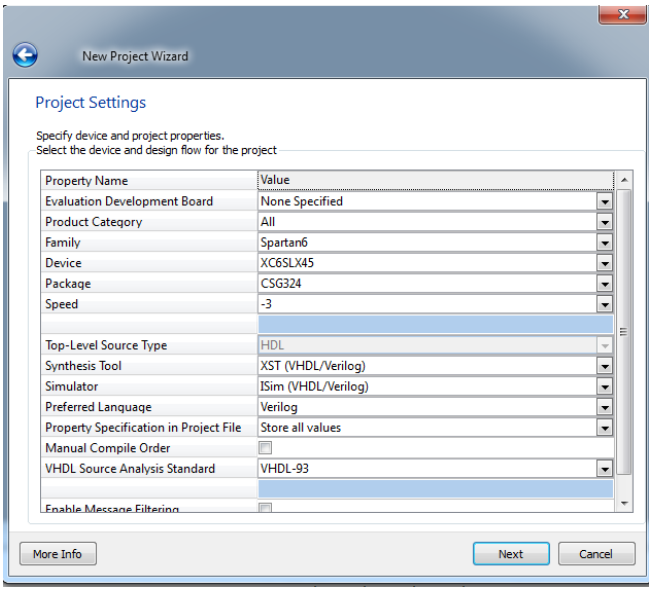
FPGAs are becoming more sophisticated, and their applications are expanding as they become more capable. When doing calculations that can be made in parallel, the FPGAs are programmed to deal specifically with this problem. Because of the high speed I/O capabilities of the FPGA, it is ideal for acceleration of certain problems.

II. INSTALLING SOFTWARE

While we use Xilinx Foundation 4 in lab, Xilinx has changed their development to ISE Foundation, which has enhanced capabilities for place-and-route, as well as more robust verification, timing, and planning tools. A free development system is available from Xilinx. ISE WebPack, is currently at version 14.4, and is available for Windows and Linux.
The software should already be installed on the computers in the lab, but it also available from xlinx.com under "downloads"

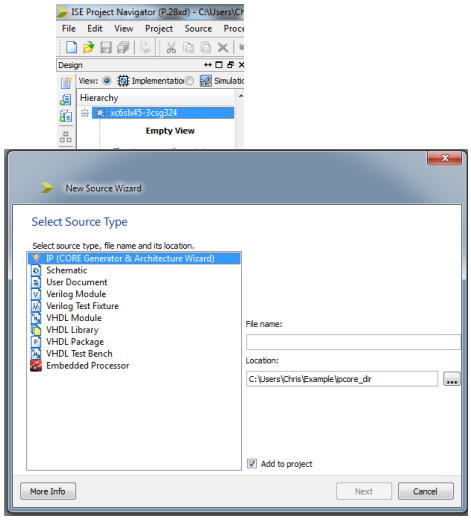
III. USING XILINX ISE PROJECT NAVIGATOR

a. Start program called "ISE Project Navigator. This may not be on desktop but under the Programs folder in the Start Menu.
b. Create a new project.

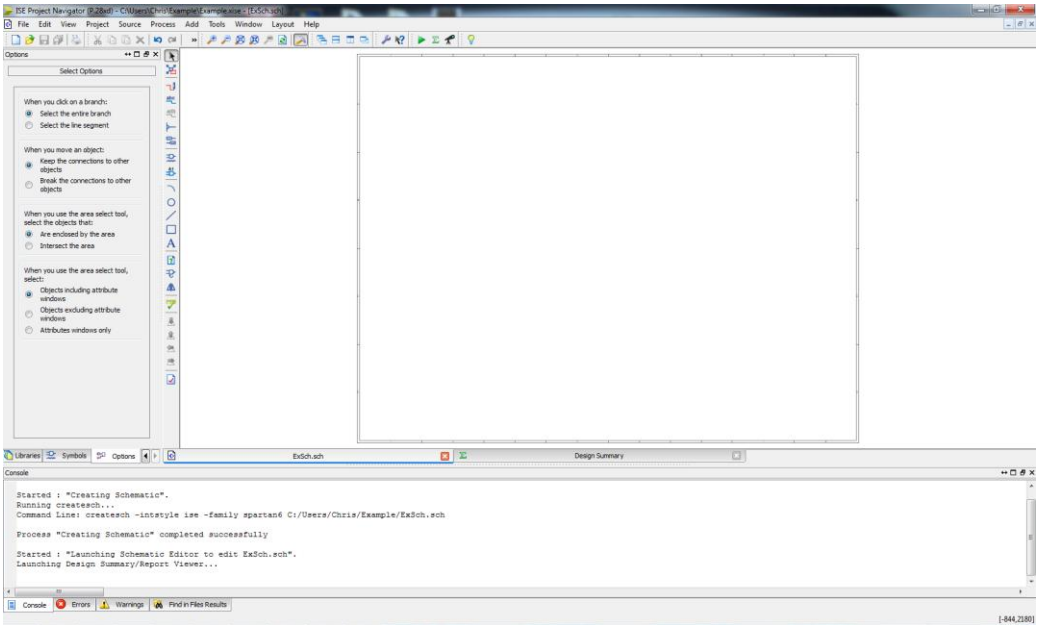


c. Name the project, select a file path to save it in and select your top level source type (for this example we will use "Schematic")
d. Select "Spartan" in the "Family" box, "XC6SLX45" in the device box and "CSG324" in the "Package" box
e. When the "Project Summary" box appears, select "Finish"

f. Click on “XC6SLX45” in the design hierarchy window on the left of the screen, then click the bh “new source” button just above and to the left

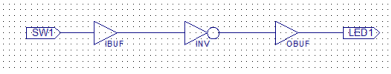


g. When the “Select Source Type” window appears, select “Schematic” and enter a name for the source fileOnce the grid appears you must select parts for your schematic. Most of the time, you will be using the “Draw Wires”, “Symbols Toolbox” and “Add IO Toolbox”

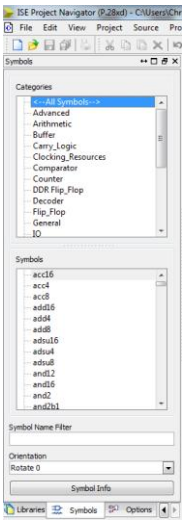


h. Like Pspice, the Symbol tool lets you add parts by connecting the respective **leads** together with the mouse or with the wire drawing tool. After clicking the parts button

- **i.** Every Input *must* be followed by **IBUF**
- **ii.** Every Output *must* be preceded by **OBUF**

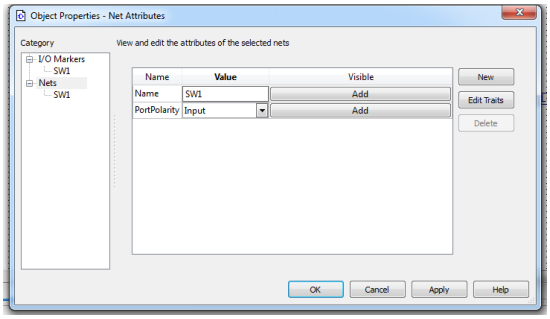


iii. ***Input(s) & Output(s):*** Must be assigned **PIN LOCALIZATION NUMBERS**. (see step l)



i. Inputs and outputs should be named in such a way to help illustrate their purpose

i. To input a name, double click on the symbol, click "Nets" in the category on the left of the window that appears and type the desired name in the value field under the "Name" row



j. Assigning pin locations

i. Create a constraint file by clicking on the "design" at the bottom of the design window (if the tap is not visible click the arrows in the bottom right corner of the window to scroll through the different tabs)

ii. Select your schematic in the hierarch window

iii. Click the "New Source" button

iv. Select the "implementation constraint file" under "source type" and input a name

v. To assign a pin to an input/output, type "**NET "<**`block name>`**" LOC="**`<pin location>`**";**" into the text file that was created when

you created the constraint file

Pushbuttons	Slide Switches	LEDs
BTNU: N4	SW0: A10	LD0: U18
BTNC: F5	SW1: D14	LD1: M14
BTNR: F6	SW2: C14	LD2: N14
BTNL: P4	SW3: P15	LD3: L14
BTND: P3	SW4: P12	LD4: M13
BRST: T15	SW5: R5	LD5: D4
	SW6: T5	LD6: P16
	SW7: E4	LD7: N12

Important Pin Locations (for full list see Appendix A)

IV. IMPLEMENTATION/PROGRAMMING

a. After the circuit is simulated and working properly you can than proceed to implement your circuit on the FPGA.
b. First make sure that the FPGA is properly connected (parallel and power cables).
c. Click on the "Implement" button (green arrow on the middle left of the design window)
d. The next step is to download the circuit into the FPGA. To accomplish this press the Programming button, select iMPACT and press OK.

V. APPENDIX A: FULL PIN LISTING

Device/Package 6slx45csg324 Wed Mar 31 17:26:12 2010

Pin	Bank	BUFIO2	Pin Description
D4	0	TL	IO_L1P_HSWAPEN_0
C4	0	TL	IO_L1N_VREF_0
B2	0	TL	IO_L2P_0
A2	0	TL	IO_L2N_0
D6	0	TL	IO_L3P_0
C6	0	TL	IO_L3N_0
B3	0	TL	IO_L4P_0
A3	0	TL	IO_L4N_0
B4	0	TL	IO_L5P_0
A4	0	TL	IO_L5N_0
C5	0	TL	IO_L6P_0
A5	0	TL	IO_L6N_0
C7	0	TL	IO_L10P_0
A7	0	TL	IO_L10N_0
B6	0	TL	IO_L8P_0
A6	0	TL	IO_L8N_VREF_0
D8	0	TL	IO_L11P_0
C8	0	TL	IO_L11N_0
B8	0	TL	IO_L33P_0
A8	0	TL	IO_L33N_0
D9	0	TL	IO_L34P_GCLK19_0
C9	0	TL	IO_L34N_GCLK18_0
B9	0	TL	IO_L35P_GCLK17_0

A9	0	TL	IO_L35N_GCLK16_0
D11	0	TR	IO_L36P_GCLK15_0
C11	0	TR	IO_L36N_GCLK14_0
C10	0	TR	IO_L37P_GCLK13_0
A10	0	TR	IO_L37N_GCLK12_0
G9	0	TR	IO_L38P_0
F9	0	TR	IO_L38N_VREF_0
B11	0	TR	IO_L39P_0
A11	0	TR	IO_L39N_0
B12	0	TR	IO_L41P_0
A12	0	TR	IO_L41N_0
C13	0	TR	IO_L50P_0
A13	0	TR	IO_L50N_0
B14	0	TR	IO_L62P_0
A14	0	TR	IO_L62N_VREF_0
F13	0	TR	IO_L63P_SCP7_0
E13	0	TR	IO_L63N_SCP6_0
C15	0	TR	IO_L64P_SCP5_0
A15	0	TR	IO_L64N_SCP4_0
D14	0	TR	IO_L65P_SCP3_0
C14	0	TR	IO_L65N_SCP2_0
B16	0	TR	IO_L66P_SCP1_0
A16	0	TR	IO_L66N_SCP0_0
A17	NA	NA	TCK
D15	NA	NA	TDI
B18	NA	NA	TMS
D16	NA	NA	TDO
F15	1	RT	IO_L1P_A25_1
F16	1	RT	IO_L1N_A24_VREF_1
C17	1	RT	IO_L29P_A23_M1A13_1
C18	1	RT	IO_L29N_A22_M1A14_1
F14	1	RT	IO_L30P_A21_M1RESET_1
G14	1	RT	IO_L30N_A20_M1A11_1
D17	1	RT	IO_L31P_A19_M1CKE_1
D18	1	RT	IO_L31N_A18_M1A12_1
H12	1	RT	IO_L32P_A17_M1A8_1
G13	1	RT	IO_L32N_A16_M1A9_1
E16	1	RT	IO_L33P_A15_M1A10_1
E18	1	RT	IO_L33N_A14_M1A4_1
K12	1	RT	IO_L34P_A13_M1WE_1
K13	1	RT	IO_L34N_A12_M1BA2_1
F17	1	RT	IO_L35P_A11_M1A7_1
F18	1	RT	IO_L35N_A10_M1A2_1
H13	1	RT	IO_L36P_A9_M1BA0_1
H14	1	RT	IO_L36N_A8_M1BA1_1
H15	1	RT	IO_L37P_A7_M1A0_1
H16	1	RT	IO_L37N_A6_M1A1_1
G16	1	RT	IO_L38P_A5_M1CLK_1
G18	1	RT	IO_L38N_A4_M1CLKN_1
J13	1	RT	IO_L39P_M1A3_1
K14	1	RT	IO_L39N_M1ODT_1
L12	1	RT	IO_L40P_GCLK11_M1A5_1
L13	1	RT	IO_L40N_GCLK10_M1A6_1
K15	1	RT	IO_L41P_GCLK9_IRDY1_M1RASN_1
K16	1	RT	IO_L41N_GCLK8_M1CASN_1
L15	1	RB	IO_L42P_GCLK7_M1UDM_1
L16	1	RB	IO_L42N_GCLK6_TRDY1_M1LDM_1

H17	1	RB	IO_L43P_GCLK5_M1DQ4_1
H18	1	RB	IO_L43N_GCLK4_M1DQ5_1
J16	1	RB	IO_L44P_A3_M1DQ6_1
J18	1	RB	IO_L44N_A2_M1DQ7_1
K17	1	RB	IO_L45P_A1_M1LDQS_1
K18	1	RB	IO_L45N_A0_M1LDQSN_1
L17	1	RB	IO_L46P_FCS_B_M1DQ2_1
L18	1	RB	IO_L46N_FOE_B_M1DQ3_1
M16	1	RB	IO_L47P_FWE_B_M1DQ0_1
M18	1	RB	IO_L47N_LDC_M1DQ1_1
N17	1	RB	IO_L48P_HDC_M1DQ8_1
N18	1	RB	IO_L48N_M1DQ9_1
P17	1	RB	IO_L49P_M1DQ10_1
P18	1	RB	IO_L49N_M1DQ11_1
N15	1	RB	IO_L50P_M1UDQS_1
N16	1	RB	IO_L50N_M1UDQSN_1
T17	1	RB	IO_L51P_M1DQ12_1
T18	1	RB	IO_L51N_M1DQ13_1
U17	1	RB	IO_L52P_M1DQ14_1
U18	1	RB	IO_L52N_M1DQ15_1
M14	1	RB	IO_L53P_1
N14	1	RB	IO_L53N_VREF_1
L14	1	RB	IO_L61P_1
M13	1	RB	IO_L61N_1
P15	1	RB	IO_L74P_AWAKE_1
P16	1	RB	IO_L74N_DOUT_BUSY_1
R16	NA	NA	SUSPEND
P13	2	NA	CMPCS_B_2
V17	2	NA	DONE_2
R15	2	BR	IO_L1P_CCLK_2
T15	2	BR	IO_L1N_M0_CMPMISO_2
U16	2	BR	IO_L2P_CMPCLK_2
V16	2	BR	IO_L2N_CMPMOSI_2
R13	2	BR	IO_L3P_D0_DIN_MISO_MISO1_2
T13	2	BR	IO_L3N_MOSI_CSI_B_MISO0_2
U15	2	BR	IO_L5P_2
V15	2	BR	IO_L5N_2
T14	2	BR	IO_L12P_D1_MISO2_2
V14	2	BR	IO_L12N_D2_MISO3_2
N12	2	BR	IO_L13P_M1_2
P12	2	BR	IO_L13N_D10_2
U13	2	BR	IO_L14P_D11_2
V13	2	BR	IO_L14N_D12_2
M11	2	BR	IO_L15P_2
N11	2	BR	IO_L15N_2
R11	2	BR	IO_L16P_2
T11	2	BR	IO_L16N_VREF_2
T12	2	BR	IO_L19P_2
V12	2	BR	IO_L19N_2
N10	2	BR	IO_L20P_2
P11	2	BR	IO_L20N_2
M10	2	BR	IO_L22P_2
N9	2	BR	IO_L22N_2
U11	2	BR	IO_L23P_2
V11	2	BR	IO_L23N_2
R10	2	BR	IO_L29P_GCLK3_2
T10	2	BR	IO_L29N_GCLK2_2

U10	2	BR	IO_L30P_GCLK1_D13_2
V10	2	BR	IO_L30N_GCLK0_USERCCLK_2
R8	2	BL	IO_L31P_GCLK31_D14_2
T8	2	BL	IO_L31N_GCLK30_D15_2
T9	2	BL	IO_L32P_GCLK29_2
V9	2	BL	IO_L32N_GCLK28_2
M8	2	BL	IO_L40P_2
N8	2	BL	IO_L40N_2
U8	2	BL	IO_L41P_2
V8	2	BL	IO_L41N_VREF_2
U7	2	BL	IO_L43P_2
V7	2	BL	IO_L43N_2
N7	2	BL	IO_L44P_2
P8	2	BL	IO_L44N_2
T6	2	BL	IO_L45P_2
V6	2	BL	IO_L45N_2
R7	2	BL	IO_L46P_2
T7	2	BL	IO_L46N_2
N6	2	BL	IO_L47P_2
P7	2	BL	IO_L47N_2
R5	2	BL	IO_L48P_D7_2
T5	2	BL	IO_L48N_RDWR_B_VREF_2
U5	2	BL	IO_L49P_D3_2
V5	2	BL	IO_L49N_D4_2
R3	2	BL	IO_L62P_D5_2
T3	2	BL	IO_L62N_D6_2
T4	2	BL	IO_L63P_2
V4	2	BL	IO_L63N_2
N5	2	BL	IO_L64P_D8_2
P6	2	BL	IO_L64N_D9_2
U3	2	BL	IO_L65P_INIT_B_2
V3	2	BL	IO_L65N_CSO_B_2
V2	2	NA	PROGRAM_B_2
N4	3	LB	IO_L1P_3
N3	3	LB	IO_L1N_VREF_3
P4	3	LB	IO_L2P_3
P3	3	LB	IO_L2N_3
L6	3	LB	IO_L31P_3
M5	3	LB	IO_L31N_VREF_3
U2	3	LB	IO_L32P_M3DQ14_3
U1	3	LB	IO_L32N_M3DQ15_3
T2	3	LB	IO_L33P_M3DQ12_3
T1	3	LB	IO_L33N_M3DQ13_3
P2	3	LB	IO_L34P_M3UDQS_3
P1	3	LB	IO_L34N_M3UDQSN_3
N2	3	LB	IO_L35P_M3DQ10_3
N1	3	LB	IO_L35N_M3DQ11_3
M3	3	LB	IO_L36P_M3DQ8_3
M1	3	LB	IO_L36N_M3DQ9_3
L2	3	LB	IO_L37P_M3DQ0_3
L1	3	LB	IO_L37N_M3DQ1_3
K2	3	LB	IO_L38P_M3DQ2_3
K1	3	LB	IO_L38N_M3DQ3_3
L4	3	LB	IO_L39P_M3LDQS_3
L3	3	LB	IO_L39N_M3LDQSN_3
J3	3	LB	IO_L40P_M3DQ6_3
J1	3	LB	IO_L40N_M3DQ7_3

H2	3	LB	IO_L41P_GCLK27_M3DQ4_3
H1	3	LB	IO_L41N_GCLK26_M3DQ5_3
K4	3	LB	IO_L42P_GCLK25_TRDY2_M3UDM_3
K3	3	LB	IO_L42N_GCLK24_M3LDM_3
L5	3	LT	IO_L43P_GCLK23_M3RASN_3
K5	3	LT	IO_L43N_GCLK22_IRDY2_M3CASN_3
H4	3	LT	IO_L44P_GCLK21_M3A5_3
H3	3	LT	IO_L44N_GCLK20_M3A6_3
L7	3	LT	IO_L45P_M3A3_3
K6	3	LT	IO_L45N_M3ODT_3
G3	3	LT	IO_L46P_M3CLK_3
G1	3	LT	IO_L46N_M3CLKN_3
J7	3	LT	IO_L47P_M3A0_3
J6	3	LT	IO_L47N_M3A1_3
F2	3	LT	IO_L48P_M3BA0_3
F1	3	LT	IO_L48N_M3BA1_3
H6	3	LT	IO_L49P_M3A7_3
H5	3	LT	IO_L49N_M3A2_3
E3	3	LT	IO_L50P_M3WE_3
E1	3	LT	IO_L50N_M3BA2_3
F4	3	LT	IO_L51P_M3A10_3
F3	3	LT	IO_L51N_M3A4_3
D2	3	LT	IO_L52P_M3A8_3
D1	3	LT	IO_L52N_M3A9_3
H7	3	LT	IO_L53P_M3CKE_3
G6	3	LT	IO_L53N_M3A12_3
E4	3	LT	IO_L54P_M3RESET_3
D3	3	LT	IO_L54N_M3A11_3
F6	3	LT	IO_L55P_M3A13_3
F5	3	LT	IO_L55N_M3A14_3
C2	3	LT	IO_L83P_3
C1	3	LT	IO_L83N_VREF_3
A1	NA	NA	GND
A18	NA	NA	GND
B13	NA	NA	GND
B7	NA	NA	GND
C16	NA	NA	GND
C3	NA	NA	GND
D10	NA	NA	GND
D5	NA	NA	GND
E15	NA	NA	GND
G12	NA	NA	GND
G17	NA	NA	GND
G2	NA	NA	GND
G5	NA	NA	GND
H10	NA	NA	GND
H8	NA	NA	GND
J11	NA	NA	GND
J15	NA	NA	GND
J4	NA	NA	GND
J9	NA	NA	GND
K10	NA	NA	GND
K8	NA	NA	GND
L11	NA	NA	GND
L9	NA	NA	GND
M17	NA	NA	GND
M2	NA	NA	GND

M6	NA	NA	GND
N13	NA	NA	GND
R1	NA	NA	GND
R14	NA	NA	GND
R18	NA	NA	GND
R4	NA	NA	GND
R9	NA	NA	GND
T16	NA	NA	GND
U12	NA	NA	GND
U6	NA	NA	GND
V1	NA	NA	GND
V18	NA	NA	GND
B1	NA	NA	VCCAUX
B17	NA	NA	VCCAUX
E14	NA	NA	VCCAUX
E5	NA	NA	VCCAUX
E9	NA	NA	VCCAUX
G10	NA	NA	VCCAUX
J12	NA	NA	VCCAUX
K7	NA	NA	VCCAUX
M9	NA	NA	VCCAUX
P10	NA	NA	VCCAUX
P14	NA	NA	VCCAUX
P5	NA	NA	VCCAUX
G7	NA	NA	VCCINT
H11	NA	NA	VCCINT
H9	NA	NA	VCCINT
J10	NA	NA	VCCINT
J8	NA	NA	VCCINT
K11	NA	NA	VCCINT
K9	NA	NA	VCCINT
L10	NA	NA	VCCINT
L8	NA	NA	VCCINT
M12	NA	NA	VCCINT
M7	NA	NA	VCCINT
B10	0	NA	VCCO_0
B15	0	NA	VCCO_0
B5	0	NA	VCCO_0
D13	0	NA	VCCO_0
D7	0	NA	VCCO_0
E10	0	NA	VCCO_0
E17	1	NA	VCCO_1
G15	1	NA	VCCO_1
J14	1	NA	VCCO_1
J17	1	NA	VCCO_1
M15	1	NA	VCCO_1
R17	1	NA	VCCO_1
P9	2	NA	VCCO_2
R12	2	NA	VCCO_2
R6	2	NA	VCCO_2
U14	2	NA	VCCO_2
U4	2	NA	VCCO_2
U9	2	NA	VCCO_2
E2	3	NA	VCCO_3
G4	3	NA	VCCO_3
J2	3	NA	VCCO_3
J5	3	NA	VCCO_3

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M4        3       NA      VCCO_3
R2        3       NA      VCCO_3
E7        NOPAD/UNCONNECTED
E8        NOPAD/UNCONNECTED
F7        NOPAD/UNCONNECTED
E6        NOPAD/UNCONNECTED
G8        NOPAD/UNCONNECTED
F8        NOPAD/UNCONNECTED
G11       NOPAD/UNCONNECTED
F10       NOPAD/UNCONNECTED
F11       NOPAD/UNCONNECTED
E11       NOPAD/UNCONNECTED
D12       NOPAD/UNCONNECTED
C12       NOPAD/UNCONNECTED
F12       NOPAD/UNCONNECTED
E12       NOPAD/UNCONNECTED

Total Number of Pins generated, 324
```